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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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IP Section

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EXAMINER

RODELA, EDUARDO A

ART UNIT

PAPER NUMBER

2893

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DELIVERY MODE

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/680,578	Applicant(s) LEE ET AL.	
	Examiner EDUARDO A. RODELA	Art Unit 2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 October 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 and 49 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 and 49 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10/7/2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☐ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

DETAILED ACTION

This Office Action is in response to the communications received October 28, 2010.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the shapes which reflect the claimed integer values of claims 22-24, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-9, 11, 12, 15-18, 20, 21 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Harada et al. (Us 2002/0005583).

Regarding claim 1, Harada shows in Figure 36, a structure for corners of metallic features of semiconductor integrated circuits, comprising:

metallic features [top feature 101 and bottom feature 250], imbedded in dielectric layers [7c, 15a-d, 202a,b and 230a-d], wherein corner angles of all corners of the metallic features are greater than 90 degrees [all internal angles of features 101 and 250 are greater than 90 degrees as shown in Figure 36A and also discussed in paragraph 0258].

Regarding claim 2, Harada shows the structure of claim 1, wherein one of said dielectric layers includes a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride [paragraphs 0262, 0267 and 0271].

Regarding claim 3, Harada shows the structure of claim 1, wherein one of said dielectric layers is a composite of dielectric layers [silicon oxynitride, 202b in paragraph 0271].

Regarding claim 5, Harada shows the structure of claim 1, wherein one of said metallic features [101 and 250] includes a material of Cu [paragraphs 0266 and 0271].

Regarding claim 6, Harada shows the structure of claim 1, wherein one of said metallic features [101 and 250] is a feature selected from the group consisting of via, trench, pad [see Figures 36A&B].

Regarding claim 7, Harada shows in Figure 36, a structure for corners of metallic features of semiconductor integrated circuits, comprising:

metallic features [101 and 250], imbedded in dielectric layers [7c, 15a-d, 202a,b and 230a-d], wherein corners of all metallic features are formed in n-fold clipped corner configurations, with n being greater than 0 [all internal angles of features 101 and 250 are greater than 90 degrees as shown in Figure 36A and also discussed in paragraph 0258].

Regarding claim 8, Harada shows the structure of claim 7, wherein one of said dielectric layers includes a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride [paragraphs 0262, 0267 and 0271].

Regarding claim 9, Harada shows the structure of claim 7, wherein one of said dielectric layers is a composite of dielectric layers [silicon oxynitride, 202b in paragraph 0271].

Regarding claim 11, Harada shows the structure of claim 7, wherein one of said metallic features [101 and 250] includes a material of Cu [paragraphs 0266 and 0271].

Regarding claim 12, Harada shows the structure of claim 7, wherein one of said metallic features [101 and 250] is a feature selected from the group consisting of via, trench, pad [see Figures 36A&B].

Regarding claim 15, Harada shows the structure of claim 7, wherein said n-fold clipped corner configurations of comers of metallic features of a level are n-fold equal angle clipped corner configurations, with n equal or greater than one [shown in the previous rejection of claim

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7]; and when said dielectric layer of said level is of includes a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride [paragraphs 0262, 0267 and 0271].

It is noted that the limitation of “no CMP step is done on said level” is considered to be a process limitation that carries no patentable weight because the current claim is directed to a device structure, therefore a “product by process” claim is directed to the product, and no matter how the structure is actually made, it is the final product which must be determined in a “product by process” claim, and not the patentability of the process.

Regarding claim 16, Harada shows in Figures 36A&B and Figure 41, a structure for metallic features of semiconductor integrated circuits, comprising:

shapes of all metallic features [101 and 250] imbedded in dielectric layers [7c, 15a-d, 202a,b and 230a-d], that could be formed as squares, are instead configured as m-sided regular polygons, where m is greater than 4 [see the shape of 101 and 250 in Figure 41].

Regarding claim 17, Harada shows the structure of claim 16, wherein one of said dielectric layers includes a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride [paragraphs 0262, 0267 and 0271].

Regarding claim 18, Harada shows the structure of claim 16, wherein one of said dielectric layers is a composite of dielectric layers [silicon oxynitride, 202b in paragraph 0271].

Regarding claim 20, Harada shows the structure of claim 16, wherein one of said metallic features [101 and 250] includes a material of Cu [paragraphs 0266 and 0271].

Regarding claim 21, Harada shows the structure of claim 16, wherein one of said metallic features [101 and 250] is a pad [see Figures 36A&B].

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Regarding claim 24, Harada shows the structure of claim 16, wherein m of each said m -sided regular polygon is at least equal to 8 [see 101 and 250 of Figure 41] when said metallic features are on a level where said dielectric layer of includes a material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride [paragraphs 0262, 0267 and 0271].

It is noted that the limitation of “has a structural characteristic resulting from a CMP step” is considered to be a process limitation that carries no patentable weight because the current claim is directed to a device structure, therefore a “product by process” claim is directed to the product, and no matter how the structure is actually made, it is the final product which must be determined in a “product by process” claim, and not the patentability of the process. Further Harada does show that all metallization levels (with dielectric layers included) ultimately are flat/level/planar, and thus necessarily have the discussed structural characteristic. But since this is a structure claim, the planarity does not need to arise from CMP processing, but must merely be present.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4, 10, 13, 14, 21-23 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. (US 2002/0005583) in view of Hung et al. (US 2003/0020163).

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Regarding claim 4, Harada shows the structure of claim 1. Harada does not show wherein one of said dielectric layers is a low-K dielectric material. Hung shows in Figure 2C, wherein one of said dielectric layers [204, 206, 210, 212 and 216, paragraph 0029] is a low-K dielectric material [paragraph 0029].

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used wherein one of said dielectric layers is a low-K dielectric material in the invention of Harada as taught by Hung, for the purpose of improving the performance of the overall device by decreasing the RC time constant.

Regarding claim 10, Harada shows the structure of claim 7. Harada does not show wherein one of said dielectric layers is a low-K dielectric material. Hung shows in Figure 2C, wherein one of said dielectric layers [204, 206, 210, 212 and 216, paragraph 0029] is a low-K dielectric material [paragraph 0029]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used wherein one of said dielectric layers is a low-K dielectric material in the invention of Harada as taught by Hung, for the purpose of improving the performance of the overall device by decreasing the RC time constant.

Regarding claim 13, Harada shows the structure of claim 7, wherein said n-fold clipped corner configurations of comers of metallic features of a level are n-fold equal angle clipped corner configurations, with n equal or greater than one [shown in the previous rejection of claim 7]. Harada does not discuss wherein when said dielectric layer of said level is a low-K dielectric material.

Hung shows in Figure 2C, wherein when said dielectric layer of said level [204, 206, 210, 212 and 216, all levels shown as low-K, paragraph 0029] is a low-K dielectric material

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[paragraph 0029]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used wherein when said dielectric layer of said level is a low-K dielectric material in the invention of Harada as taught by Hung, for the purpose of improving the performance of the overall device by decreasing the RC time constant.

It is noted that the limitation of “no CMP step is done on said level” is considered to be a process limitation that carries no patentable weight because the current claim is directed to a device structure, therefore a “product by process” claim is directed to the product, and no matter how the structure is actually made, it is the final product which must be determined in a “product by process” claim, and not the patentability of the process.

Regarding claim 14, Harada shows the structure of claim 7, wherein said n-fold clipped corner configurations of comers of metallic features of a level are n-fold equal angle clipped corner configurations, with n equal or greater than 2 [shown Figure 41, which is an alternative embodiment of shapes for 101 and 250, see paragraph 0277]. Harada does not discuss wherein when said dielectric layer of said level is a low-K dielectric material.

Hung shows in Figure 2C, wherein when said dielectric layer of said level [204, 206, 210, 212 and 216, all levels shown as low-K, paragraph 0029] is a low-K dielectric material [paragraph 0029]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used wherein when said dielectric layer of said level is a low-K dielectric material in the invention of Harada as taught by Hung, for the purpose of improving the performance of the overall device by decreasing the RC time constant.

It is noted that the limitation of “no CMP step is done on said level” is considered to be a process limitation that carries no patentable weight because the current claim is directed to a

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device structure, therefore a “product by process” claim is directed to the product, and no matter how the structure is actually made, it is the final product which must be determined in a “product by process” claim, and not the patentability of the process.

Regarding claim 21, Harada shows the structure of claim 16. Harada does not show wherein one of said dielectric layers is a low-K dielectric material. Hung shows in Figure 2C, wherein one of said dielectric layers [204, 206, 210, 212 and 216, paragraph 0029] is a low-K dielectric material [paragraph 0029].

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used wherein one of said dielectric layers is a low-K dielectric material in the invention of Harada as taught by Hung, for the purpose of improving the performance of the overall device by decreasing the RC time constant.

Regarding claim 22, Harada shows the structure of claim 16, wherein m of each said m-sided regular polygon is at least equal to 8 [see 101 and 250 of Figure 41]. Harada does not show wherein said metallic features are on a level where said dielectric layer includes a low-K dielectric material.

Harada does not discuss wherein when said dielectric layer of said level is a low-K dielectric material.

Hung shows in Figure 2C, wherein when said dielectric layer of said level [204, 206, 210, 212 and 216, all levels shown as low-K, paragraph 0029] is a low-K dielectric material [paragraph 0029]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used wherein when said dielectric layer of said level is a

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low-K dielectric material in the invention of Harada as taught by Hung, for the purpose of improving the performance of the overall device by decreasing the RC time constant.

It is noted that the limitation of “no CMP step is done on said level” is considered to be a process limitation that carries no patentable weight because the current claim is directed to a device structure, therefore a “product by process” claim is directed to the product, and no matter how the structure is actually made, it is the final product which must be determined in a “product by process” claim, and not the patentability of the process.

Regarding claim 23, Harada shows the structure of claim 16, wherein m of each said m-sided regular polygon is at least equal to 16 [see 101 and 250 of Figure 41]. Harada does not show wherein said metallic features are on a level where said dielectric layer includes a low-K dielectric material.

Harada does not discuss wherein when said dielectric layer of said level is a low-K dielectric material.

Hung shows in Figure 2C, wherein when said dielectric layer of said level [204, 206, 210, 212 and 216, all levels shown as low-K, paragraph 0029] is a low-K dielectric material [paragraph 0029]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used wherein when said dielectric layer of said level is a low-K dielectric material in the invention of Harada as taught by Hung, for the purpose of improving the performance of the overall device by decreasing the RC time constant.

It is noted that the limitation of “has a structural characteristic resulting from a CMP step” is considered to be a process limitation that carries no patentable weight because the current claim is directed to a device structure, therefore a “product by process” claim is directed

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to the product, and no matter how the structure is actually made, it is the final product which must be determined in a “product by process” claim, and not the patentability of the process. Further Harada does show that all metallization levels (with dielectric layers included) ultimately are flat/level/planar, and thus necessarily have the discussed structural characteristic. But since this is a structure claim, the planarity does not need to arise from CMP processing, but must merely be present.

Regarding claim 49, Harada/Hung show the structure of claim 4. Hung shows further wherein said dielectric layer [said “SiLK” material] has a dielectric constant less than about 3.0 [known to be lower than 3.0,].

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are not convincing.

The rejections made fully satisfy each limitation of the claims, the broadest reasonable interpretation has been made by the Examiner, which is to say that all the angle claims are fully satisfied by the shape orientation provided by the prior art. The recitation “corner angles of all corners of the metallic features” merely means that the corner angles of all of the corners of any of the given metallic structures, (several selected by the Examiner in the prior art), must have the specified angles. The prior art clearly shows this limitation.

Conclusion

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THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Fax / Telephone Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **EDUARDO A. RODELA** whose telephone number is (571)272-8797. The examiner can normally be reached on M-F, 9 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on (571)272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Evan Pert/
Primary Examiner, Art Unit 2826

EDUARDO A. RODELA /EAR/
Examiner
Art Unit 2893